Last Updated June 02, 2016

Title	**Dr.**	First Name	**Manoj**	Last Name	**Saxena**	Photograph
Designation		**Associate Professor**				
Address		**Department of Electronics** **Deen Dayal Upadhyaya College** **University of Delhi** **Karampura, New Delhi-110015, India**				
Phone No Office		**011-25458173**				
Residence		**011-28531418**				
Mobile		**09968393104**				
Email		**msaxena@ddu.du.ac.in,** **saxena_manoj77@yahoo.co.in**				
Web-Page						

Educational Qualifications		
Degree	Institution	Year
Ph.D. Electronics	**University of Delhi**	**2006**
M. Sc. Electronics	**University of Delhi**	**2000** *(Gold Medalist)*
B. Sc. (H) Electronics	**University of Delhi**	**1998**

Career Profile

- Lecturer, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi *(August 2000 - December 2005)*
- Assistant Professor, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi *(01/01/2006 – 26/08/2006)*
- Assistant Professor (Senior Lecturer), Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi *(27/08/2006 – 26/08/2009)*
- Assistant Professor (Reader), Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi *(27/08/2009 - Till Date)*
- Associate Professor, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi (27/08/2012 - Till Date)

Administrative Assignments

Year 2016 – 2017

- Convener-Research Centre
- Convener – Science Foundation
- Convener – College Research Committee
- Convener – Website Committee
- Convener – Career Counseling and Placement Cell
- Convener – India Today NIELSEN Survey Committee for Science, Commerce and Arts
- Election Officer – DDU College Alumni Election for Executive 2016-2017.
- Member – UGC XIITH Plan Grants Committee
- Member - Committee for ERP solution for paperless administrative, financial and academic management of the College

Year 2015 – 2016

- Teacher-in-Charge – Department of Electronics
- Convener-Research Centre
- Convener – Science Foundation
- Convener – College Research Committee (November 19, 2015 -)

- Convener – Website Committee
- Convener – Career Counseling and Placement Cell
- Convener-Admission Committee for Electronics
- Member- Academic Development Committee
- Member - Library Committee
- Member – Alumni Committee of College
- Member – College Research Committee (Till November 19, 2015)
- Member – College Internal Quality Assurance Cell (IQAC) (Till November 19, 2015)
- Member – College Archives Committee
- Member – UGC XIITH Plan Grants Committee
- Member – Generic Committee Allotment Committee
- Member - Screening Committee for Professor Application to outside institutions
- Member - Screening Committee for Appointing Vice-Principal of the College
- Member - Committee for ERP solution for paperless administrative, financial and academic management of the College
- Member-Time Table Committee
- Member – NIRF Committee

Year 2014 – 2015

- Teacher-in-Charge – Department of Electronics
- Convener-Research Centre
- Convener-AICTE form filling up committee
- Convener – Website Committee
- Convener – Career Counseling and Placement Cell
- Member- Academic Devlopment Committee
- Member-Library Committee
- Member – Alumni Committee of College
- Member – College Research Committee
- Member – College Internal Quality Assuarnace Cell (IQAC)
- Member – College Archives Committee
- Member – UGC XIITH Plan Grants Committee
- Member - Screening Committee for Appointing Vice-Principal of the College
- Member-Time Table Committee
- Convener-Admission Committee for Electronics

Year 2013 – 2014

- Convener – Website Committee
- Convener – Career Counseling and Placement Cell
- Member – College Archives Committee
- Member – Alumni Committee of College
- Convener- Committee for Sending Proposal to DU regarding MSME, Govt. of India.
- Member – UGC XIITH Plan Grants Committee
- Member – College NAAC Steering Committee
- Member – College Research Committee
- Member – College Internal Quality Assuarnace Cell (IQAC)

Year 2012 – 2013

- Convener – College Archives Committee
- Convener - Prospectus Committee
- Convener – Career Counseling and Placement Cell

- Member – Website Committee
- Member – Alumni Committee of College
- Member – College Committee for Antardhvani 2013, University of Delhi

Year 2011 – 2012
- Convener-Career Counseling and Placement Cell
- Member-Admission Committee
- Member – Alumni Committee of College
- Member – Departmental Technical and Purchase Committee

Year 2010 – 2011
- Convener – Placement Cell
- Member – Gandhi Study Circle, DDU College
- Member – Rajiv Gandhi Study Circle, DDU College
- Member – Alumni Committee of College
- Member – Departmental Technical and Purchase Committee
- Member – Lab. Development Committee for Labs in New Block

Year 2009 – 2010
- Convener – Aryabhatta Science Forum
- Member – Gandhi Study Circle, DDU College
- Member – Rajiv Gandhi Study Circle, DDU College
- Member - Prospectus Committee
- Member – Canteen Committee
- Member – Committee for purchase of office automation software for college
- Member – Committee for renovation of furniture for staff room, principal office and seminar room of college

Year 2008 – 2009
- Convener - Prospectus Committee
- Member –Magazine Committee
- Member – Canteen Committee
- Member - Placement Cell
- Member - Admission Committee
- Member - Website Committee
- Member – Aryabhatta Science Forum

Year 2007 – 2008
- Convener - College Prospectus Committee
- Co-Convener - Time Table Committee
- Treasurer- DDUC Teaching Staff Association
- Member - College Placement Cell
- Member - Admission Committee
- Member - Library Stock Verification Committee

Year 2006 – 2007
- Convener - College Prospectus Committee
- Member - College Placement Cell
- Member - Admission Committee
- Member - Library Stock Verification Committee
- Member - Purchase Committee

- Member - Departmental Lab. maintenance Committee

Year 2005 - 2006
- Member - Student Activity Committee
- Member - College Prospectus Committee
- Member - College Website Committee
- Member - Departmental Purchase Committee
- Member - College Infrastructure Development Committee
- Member - Proctorial Board
- Member - Aryabhatta Science Forum
- Member - Library Stock Verification Committee
- Member - Admission Committee
- Member - Purchase Committee
- Treasurer- DDUC Teaching Staff Association

Year 2004 - 2005
- Member - Technical Library Purchase Committee.
- Member - Library Stock Verification Committee
- Member - Departmental Technical Committee
- Member - Departmental Time Table Committee
- Member - Student Activity Committee
- Member - Prospectus Committee
- Member - Website Development Committee

Year 2003 - 2004
- Member - Technical purchase Committee
- Member - Discipline Committee
- Member - Sports Committee

Areas of Interest / Specialization

Modeling and simulation of sub-100 nm MOSFET structures:
- Epitaxial Channel and Drain Engineered
- Dual/ Tripple Material Gate (DMG/ TMG)
- Silicon on Nothing (SON)
- Insulated Shallow Extension (ISE)
- Recessed Channel/ Grooved/ Concave Gate
- Tunnel FET
- Optically Controlled FET (OPFET)
- Mercuric Iodide (HgI_2) X-Ray Detectors

Subjects Taught

Post Graduate Level (*As Visiting Faculty*)

Course	Year
M. Sc Electronics (IVth Semester)	Jan 2013 – April 2013
VLSI Circuit Design and Device Modelling – 4.2	Jan 2012 – April 2012
(Deptt. Of Electronic Science, University of Delhi South Campus)	January 2011 – April 2011

M. Sc Electronics (I[st] Semester) Advance Analog and Digital Electronics - 1.4 *(Deptt. Of Electronic Science, University of Delhi South Campus)*	July 2012 – December 2012 July 2011 – December 2011 July 2010 – December 2010 July 2009 – December 2009 July 2008 – December 2008 July 2005 – December 2005 July 2004 – December 2004
M. Sc Informatics – Introduction to Communication Systems – IT-13 *(Institute of Informatics & Communication, University of Delhi South Campus)*	2005-2006

Under Graduate Level

Course	Year
B. Sc. (H) Electronics I Semester – Applied Physics	January 2016 – April 2016
B. Sc. (H) Electronics I Semester – Mathematics Foundation for Electronics	July 2015-November 2015
B. Tech Electronics (FYUP) - III Semester – Analog Electronics-I	July 2014-November 2014
B. Tech Electronics (FYUP) – II Semester – Semiconductor Devices	January 2014-April 2014
B. Sc. (H) Electronics III Semester – Analog Electronics-I	July 2013-November 2013 July 2012-November 2012 July 2011-November 2011
B. Sc. (H) Electronics II Semester – Signal and Systems	January 2015-April 2015 January 2013-April 2013 January 2012-April 2012 January 2011-April 2011
B. Sc. (H) Electronics III Semester – Analog Electronics-I	July 2011-November 2011
B. Sc. (H) Electronics I Semester – Network Analysis	July 2010-November 2010
B. Sc. (H) Electronics I year – Network Analysis and Linear Active circuits	2007-2010 2002-2005
B. Sc. (H) Electronics II year – Operational Amplifier and Analog Computation	2005-2010
B. Sc. (H) Electronics II year – Numerical analysis and FORTRAN programming	2007-2009
B. Sc. (H) Electronics III year – Engineering Drawing	2003-2004
B. Sc. (H) Electronics III year – Power Electronics	2005-2007
B. Sc. (H) Electronics III year – Communication System	2002-2004
B. Sc (H) Computer Science I semester - Digital Electronics	2004-2007
B. Sc (H) Computer Science II semester - Analog Electronics	2003-2004
B. Sc (H) Computer Science V semester - Microprocessor	2003-2005

Research Guidance

List against each head (If applicable)

Supervision of awarded Doctoral Thesis	One
Supervision of Doctoral Thesis, under progress	Two
Supervision of awarded M.Phil dissertations	Three
Supervision of M.Phil dissertations, under progress	Nil

Research Guidance/ Supervision

Joint Supervision

S. No.	Title	Candidate's name and Affiliation	Year	Status
•	Modeling and simulation of Nanoscale Dual Material Gate Insulated Shallow Extension Silicon on Nothing MOSFET for Low voltage low power applications	Ms. Vandana Kumari, Research Scholar, UGC-NET (LS) Department of Electronic Science, University of Delhi South Campus, New Delhi.	2010 - 2012	Awarded
•	Analytical Modeling and Simulation Study of BioFETs for Label Free Electrical Detection of Biomolecules	Mr. Ajay Research Scholar, UGC-NET-JRF Department of Electronic Science, University of Delhi South Campus, New Delhi.	July-2013	On-Going
•	Modeling and Simulation of Steep Subthreshold Emerging Research Devices for Energy Efficient Low Power Sensing Applications	Mr. Avshesh Research Scholar, UGC-NET Department of Electronic Science, University of Delhi South Campus, New Delhi.	Nov-2015	On-Going

Supervision of M. Phil dissertation

Name of the Candidate	Title of the Dissertation	University/ Roll. No.	Year/ Status
Ms. Rakhi Narang	A Gate-Induced Drain-Leakage Current Model for Fully Depleted Double-Gate MOSFETS	Reg. No – 605011080014	2009/ Awarded
Ms. Sonia Ahlawat	Modeling and Analysis of Body Potential of Cylindrical Gate-All-Around Nanowire Transistor	Reg. No -605011080015	2009/ Awarded
Ms. Neha	Microwave Modeling and Parameter extraction method for Quantum Well Laser	Reg. No – C8HR016M1250029	2009/ Awarded

Project Guidance/ Supervision

At National Level

(Summer Research Fellowship Sponsored by Indian Academy of Sciences (IAS), National Academy of Sciences, India (NASI) & Indian National Science Academy (INSA))

S. No.	Title	Candidate's name and Affiliation	Duration	Status
1.	Computer Aided Analysis, Charecterization, Optimization and Simulation of Bio-Molecules of Field Effect Biosensors	Jagriti Mishra B. Tech, BITS Meshra (ENGS1368)	May-July2010	Completed
2.	Analytical modeling and Simulation of Short Channel Effects and Quantum-Confinement Effects in	Gaurav Mahajan B.E. (Hons.) Electrical and Electronics Engineering	May-July2010	Completed

	Silicon Nanowire MOSFET	Birla Institute of Technology and Science, Pilani (ENGS2982)		
3.	Analytical modeling and Simulation of Germanium on Insulator MOSFET for Optical Application	Neha Bhushan KIIT University, Bhubaneswar (ENGS2269)	May-July2011	Completed
4.	Analytical modeling and simulation of Tunnel FET for Sensor application	K V Sasidhar Reddy NIT, Warangal (ENGS4147)	May-July2011	Completed
5.	Modeling and Application of Gate Material Engineered Double Gate Junction-Less Field Effect Transistor for Low-Voltage Low-Power Analog and Digital Circuits	Neel Modi (ENGS7096) Electronics and Communication Engineering Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat	May-July2013	Completed
6.	Logic Circuit design analysis and performance comparison of CMOS with Steep Subthreshold Devices,	Pranav P Nair, (ENGS 5351) B. Tech III Year, Electrical Engineering, IIT Indore, India	May-July2013	Completed
7.	Modeling and Simulation of Nanoscale Multi-Gate MOSFET architectures for Digital and Analog Applications	I. Aravindan ENGS 3571 B.Tech Electronics and Communication Engineering (III Year) Amrita Vishwa Vidyapeetham, Coimbatore, Tamil Nadu	May-July2014	Completed
8.	Modeling of Tapered Gate Electrode Reconfigurable Double Gate MOSFET incorporating Friging Field Effects	Gokulnath R. ENGS 3099 B.E.III Year Electrical and Electronics Engineering Sri Sai Ram Engineering College Chennai-44	May-July2015	Completed
9.	Novel Attributes of Tunnel Field Effect Transistors over conventional FET based devices	Sakshi Gupta ENGS 6707 Electronics and Communication Engineering ITM University, Gurgaon, Haryana	May-July2015	Completed
10.	Impact of Gate Underlap Region on the Electrostatistics of FINFET Architecture using Efficient 3D Analytical Model	Sharmetha K. ENGS 9097 Electronics and Communication Engineering K.S.Rangaswamy College of Technology Namakkal, Tamil Nadu, India	May-July2015	Completed

At College Level

Under Graduate Students (As Guide): 09

S. No.	Title	Candidate's name and Affiliation	Year
1.	Implementation of a Nanoelectronic Full Adder and Nano-circuit to control millimeter scale walking robot	Sumit Jain B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2007
2.	HeRMES: High-Performance Reliable MRAM-Enabled Storage and On-chip MRAM as a High-Bandwidth, Low-Latency Replacement for DRAM Physical Memories	Angad Singh B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2007
3.	Banked Microarchitectures for Complexity-Effective Superscalar Microprocessors	Gaurav Arora B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2007
4.	Handwriting Recognition Using Artificial Neural Networks	Sagar Rangra B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008
5.	Data And Picture Encryption Using Image Processing	Ankit Bhatia B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008
6.	Pattern Recognition	Preeti Duhan B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008
7.	Expert System Architecture	Garima Arora B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008
8.	Neural Networks	Saarthak Shandilya B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008
9.	Survivability on unbounded networks	Ashish Arora B. Sc. (H) Computer Science- Sixth Semester Deen Dayal Upadhyaya College, University of Delhi	2008

Publications Profile

Total Publications: **228** ***(as on May 21, 2016)***

International Refereed Journals	**085**
Conference Proceedings	**069**
Abstracts in Conferences	**074**

International Journals where my papers have been published ***(ISI Thomson Impact Factor: AS ON December 05, 2015)***

S. No.	Publication title	Impact factor	No. of Papers
1.	IEEE Transactions on Electron Devices, USA	2.472	16
2.	IEEE Transactions on Device and Material Reliability, USA	1.890	03
3.	IEEE Electron Device Letter, USA	2.754	02
4.	IEEE Transactions on Nanotechnology, USA	1.825	05
5.	Semiconductor Science Technology, Institute of Physics (IOP), UK	2.190	06
6.	Microelectronic Engineering, Elsevier, UK	1.197	02
7.	Superlattices and Microstructures, Elsevier, UK	2.097	06
8.	Solid-state Electronics, Elsevier, UK	1.504	04
9.	IEE Electronics Letters, UK	0.930	01
10.	Microwave and Optical Technology Letter, Wiley	0.568	02
11.	Microelectronics Reliability, *Elsevier, UK*	1.433	06
12.	Microelectronics Journal, *Elsevier, UK*	0.836	01
13.	International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, Wiley	0.615	01
14.	Journal of Semiconductor Science and Technology (JSTS)	0.515	07
15.	Journal of Nano- Electron. Physics	0.194	01
16.	IETE Journal of Research	0.185	02
17.	Journal of Computational and Theoretical Nanoscience (CTN)	--	03
18.	Journal of Nano Research	--	02
19.	Advanced Science, Engineering and Medicine	--	02
20.	AIP Conference Proceedings	--	01
21.	Proc. SPIE	--	03
22.	International Journal of High Speed Electronics and Systems (IJHSES)	--	01
23.	International Journal of Microwave and Optical Technology Letter (IJMOT)	--	02
24.	Communications in Computer and Information Science	--	02
25.	International journal of VLSI design & Communication Systems (VLSICS)	--	02
26.	Invertis Journal of Science and Technology	--	02

Total Citations : **365**
ORCID Webpage : http://orcid.org/0000-0002-9368-4194
Scopus Webpage : http://www.scopus.com/authid/detail.url?authorId=35480023200
ResearcherID-Thomson Reuters : http://www.researcherid.com/rid/K-3863-2015

H-Index : 11

S. No.	Title of the Journal, Vol, Issue, Page No. etc	Citation (excl. self citations)
1.	IEEE Transaction on Electron Devices, Vol. 49, No. 11, pp. 1928-1938, November 2002	62
2.	IEE Electronics Letter, 9th January, Vol. 39, No.1, pp-155-157, January 2003	15
3.	Solid State Electronics, Vol. 47, pp. 2131-2134, 2003.	14
4.	Solid State Electronics Vol. 48, pp. 1169-1174, 2004.	29
5.	IEEE Transaction on Electron Devices, Vol. No. pp. 23-29, January 2005	29
6.	IEEE Transactions on Electron Devices, Vol. 53, No. 7, pp. 1623-1633, July 2006.	28
7.	IEEE Transactions on Electron Devices, Vol. 55, No. 1, pp. 372-381, January 2008.	12
8.	Journal of Semiconductor Science and Technology, Vol.12, No.4, pp. 482-491, 2012	12
9.	IEEE Transactions on Electron Devices, Vol. 59, No. 10, pp. 2809-2817, October 2012	13
10.	IEEE Transactions on Electron Devices, Vol. 60, No. 6, pp. 1820-1827, June 2013	15
11.	Microelectronics Journal, Volume 44, Issue 6, pp. 479–488, June 2013.	12

Invited Talk Delivered:

1. "**Applications of Quantum Mechanics in Nanoscale Electronics**", Second National Workshop On Quantum Mechanics: Theory and Application Organized By FiDAS, Deen Dayal Upadhyaya College, University of Delhi, Sponsored By CSIR, Govt of India Supported By IEEE EDS Delhi Chapter, New Delhi and The National Academy of Sciences, India, - Delhi Chapter held during October 22-23, 2010 and October 29-30, 2010.
2. "**Applications of Quantum Mechanics in Nanoscale Electronics: Size Quantization Effect**", Physics Workshop organized by Kendriya Vidyalaya, R. K. Puram, Sector-2, New Delhi from December 24, 2010 to January 02, 2011
3. **"Quantum Mechanics for Nanoelectronics"** in Continuing Education Program (CEP) on "Nanoelectronics" from 17th – 21st January 2011 organized by Solid State Physics Laboratory, (laboratory under the Defence Research & Development Organization (DRDO), Govt. of India)
4. ***"Tunnel Field Effect Transistor – A Biomolecule Sensor",*** Twenty Third Meeting of Indian Academy of Sciences, Bangalore held during 13th - 14th, July 2012.
5. *Delivered Invited talk on "Information Handling"*on May 24, 2013 during First Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during May 23-25, 2013
6. *Delivered Invited talk on "Information Handling"* on May 29, 2013 during Second Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during May 28-30, 2013
7. *Delivered Invited talk on "Information Handling"* on June 05, 2013 during Third Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during June 04-06 , 2013
8. *Delivered Invited talk on "Information Handling"* on June 13, 2013 during Fourth Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during June 12-14, 2013
9. *Delivered Invited talk on "Information Handling"* on June 29, 2013 during Orientation Programme (OR-74) organized

by CPDHE, University of Delhi during June 20, 2013 – July 17, 2013

10. Delivered Invited Talk on " Information Technology" on July 17, 2013 during Master Class for First Year Students of different colleges of DU admitted under FYUP 2013 organized by CPDHE-ILLL, University of Delhi. The Master Classes for the Foundation Courses will bring 40 first year students from a few colleges for an Introductory session on 15 July (getting to know the university), to be followed by two days of intensive classes on 16 and 17 July for seven Foundation Courses.
11. Delivered Invited talk on "Information Handling" on July 27, 2013 during Fifth Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during July 26, 2013 - July 29, 2013
12. Delivered Invited talk on "Information Handling" on January 19, 2014 during Sixth Orientation Programme for Teachers of the Foundation Course – Information Technology organized by CPDHE-ILLL, University of Delhi during January 18 , 2014 - January 19, 2014
13. Delivered Invited talk on ELECTRONICS: THE SECOND SUNRISE at Three Days Workshop for PGT organized by Bal Bharti Public School (Pitampura) Training Centre, May 18-20, 2015 (Duration of the Talk: 3 Hours)
14. Delivered Invited talk on "Development and Career Opportunities in Photonics" on Einstein Day celebrated at Bal Bharti Public School (Dwarka) on July 27, 2015 (Duration of the Talk: 1 Hour)
15. Delivered Invited Talk on "Impact of Dielectric Pocket on Different Gate Geometry MOSFET Architectures for Improved Analog and Digital Performance: Modeling and Simulation" in 2nd International Conference on Science, Technology and Management, Delhi University, Conference Centre, New Delhi on September 27, 2015 (Duration of the Talk: 30 Min)
16. Delivered Invited Talk on "Tunnel Field Effect Transistor and its Application as Highly Sensitive and Fast Biosensor" in National Conference on Recent Advances in Material& Field Theory (NCRAMFT-2K15) held during December 28-29, 2015 at Bhagwan Parshuram Institute of Technology, PSP Area-4, Sector-17, Rohini Delhi. ISBN: 978-93-5254-054-9
17. Delivered Invited Talk on "Einstein and His Contributions & Career Opportunities in Photonics and Challenges in Electronic Devices" at INSPIRE Camp held during February 02, 2016 at Rajdhani College, University of Delhi (Duration 1 Hour)

Other publications (Edited works, Book reviews, Festschrift volumes, etc.)

- **Member - Editorial Board -** Proceedings of 16th Asia Pacific Microwave Conference 2004, Department of Electronic Science, University of Delhi, Allied Publishers Pvt. Ltd. 2004, ISBN 81-7764-722-9.
- ***Proceeding Editor -*** National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2006) from 22nd March – 25th March 2006, Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India, ISBN: 81-8424-026-0
- ***E-Proceeding Editor -*** National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008) from 26th September – 28th September 2008, Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India
- ***Editor*** – Proceeding of the International Symposium on Microwave and Optical Technology (ISMOT)-2009, December 16-19, 2009.
- ***Proceeding Editor -*** Third National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2010) held during January 30-31, 2010, Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India, *sponsored By University Grants Commission (UGC), Govt. of India*

Book

- "Information Technology", D. V. Singh, Shailender Kumar, Neeraj Tyagi, Pankaj Tyagi, Sanjeev Singh, **Manoj Saxena** and Ranjan Kumar, Universities Press, ISBN 9788173719004 (2013)

Research papers published in Refereed/Peer Reviewed Journals

Papers published in International Journals: -

2002

1. Physics Based Analytical Modeling of Potential and Electrical Field Distribution in Dual Material Gate (DMG)-MOSFET for Improved Hot Electron Effect and Carrier Transport Efficiency, **Manoj Saxena**, Subhasis Haldar, Mridula Gupta, and R. S. Gupta, IEEE Transaction on Electron Devices, Vol. 49, No. 11, pp. 1928-1938, November 2002. DOI: 10.1109/TED.2002.804701 ISSN : 0018-9383

2003

2. Physics Based Modeling and Simulation of Dual Material Gate Stack (DUMGAS) MOSFET, **Manoj Saxena**, Subhasis Haldar, Mridula Gupta and R. S. Gupta, IEE Electronics Letter, 9th January, Vol. 39, No.1, pp-155-157, January 2003. Online ISSN 1350-911X, Print ISSN 0013-5194

3. Modeling and simulation of asymmetric gate stack (ASYMGAS)-MOSFET, **Manoj Saxena**, Subhasis Haldar, Mridula Gupta and R. S. Gupta, Solid State Electronics, Vol. 47, pp. 2131-2134, 2003. ISSN: 0038-1101

2004

4. Design considerations for novel device architecture: Hetro -Material Double-Gate (HEM-DG) MOSFET with sub – 100 nm gate length **Manoj Saxena**, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Solid State Electronics Vol. 48, pp. 1169-1174, 2004. ISSN: 0038-1101

5. Optimization of Gate stack MOSFETs with Quantization effects, Tina Mangla, Amit Sehgal, **Manoj Saxena**, Subhasis Haldar, Mridula Gupta and R. S. Gupta, Journal of Semiconductor Science and Technology (JSTS), Vol.4, No.3, pp. 228-239, September 2004. ISSN 1598-1657 (Print) ISSN 2233-4866 (Online)

6. Two-Dimensional Analytical Modeling and Simulation of Retrograde doped HMG MOSFET, Kirti Goel, **Manoj Saxena**, Mridula Gupta and R.S. Gupta, International Journal of High Speed Electronics and Systems, Vol.14, No.3, pp.676-683, September 2004. Print ISSN: 0129-1564, Online ISSN: 1793-6438

2005

7. Two-Dimensional Analytical Threshold Voltage Model for Dual Material Gate (DMG) Epi-MOSFET, Kirti Goel, **Manoj Saxena**, Mridula Gupta and R.S. Gupta, IEEE Transactions on Electron Devices, Vol.52, No.1, pp.23-29, January 2005. ISSN : 0018-9383

8. Physics-based algorithm implementation for characterization of gate dielectric engineered MOSFETs including Quantization effects, Tina Mangla, Amit Sehgal, **Manoj Saxena**, Subhasis Haldar, Mridula Gupta and R. S. Gupta, Journal of Semiconductor Science and Technology (JSTS), Vol.5, No.3, pp.69-77, September 2005. ISSN 1598-1657 (Print) ISSN 2233-4866 (Online)

9. Modeling and Simulation of Stacked Gate Oxide (STGO) Architecture in Silicon-On-Nothing (SON) MOSFET Poonam Kasturi, **Manoj Saxena** and R.S. Gupta, Solid State Electronics, Vol. 49, No. 10, pp. 1639-1648,October 2005. ISSN: 0038-1101

2006

10. Modeling and Simulation of a Nanoscale Three Region Tri MAterial Gate Stack (TRIMGAS) MOSFET for Improved Carrier Transport Efficiency and Reduced Hot Electron Effects, IEEE Transactions on Electron Devices, Kirti Goel, **Manoj Saxena**, Mridula Gupta and R. S. Gupta, Vol. 53, No. 7, pp. 1623-1633, July 2006. ISSN : 0018-9383

11. Two-Dimensional Analysis and Simulation for Gate Stack Silicon-On-Nothing MOSFET (GAS-SON MOSFET), Poonam Kasturi, **Manoj Saxena**, R.S. Gupta, International Journal of Microwave and Optical Technology Letter (IJMOT), Vol. 1, No. 2, pp. 417-421, August 2006. ISSN 1553-0396

2007

12. Performance Investigation of 50nm Insulated Shallow Extension Gate Stack (ISEGaS) MOSFET for Mixed Mode Applications, Ravneet Kaur, Rishu Chaujar, **Manoj Saxena** and R. S. Gupta, IEEE Transactions on Electron Devices, Vol. 54, No.2, pp. 365-368, February 2007. ISSN : 0018-9383

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15. SiGe Metal Semiconductor Field Effect Transistor (MESFET) Photodectetor Having Tailorable Photoresponse Using Bandgap Engineering, Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **International Conference on Materials for Advance Technologies, (ICMAT 2011),** June 26, 2011 – July 01, 2011, Singapore (ABSTRACT appeared in Proceedings)
16. Simulation Study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for High Temperature Applications, Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **International Conference on Materials for Advance Technologies, (ICMAT 2011),** June 26, 2011 – July 01, 2011, Singapore(ABSTRACT appeared in Proceedings)
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19. Study of Performance Degradation of the Nanoscale Cylindrical Surrounding Gate MOSFET due to Hot Carrier Induced Localized Charges, Rajni Gautam, **Manoj Saxena,** Mridula Gupta and R. S. Gupta, **International Conference on Latest Trends in Nanoscience and Nanotechnology (ICNSNT),** 28th -29th March 2011, Karnataka, India
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21. Effect of Temperature and Gate Stack on the Linearity and Analog Performance of Double Gate Tunnel FET, Rakhi Narang, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **The Second International Workshop on VLSI (VLSI 2011) in conjunction with (NECOM-2011)**, Venue: The Park Hotels, July 15 ~ 17, 2011, Chennai, India.
22. Channel Material Engineered Nanoscale Cylindrical Surrounding Gate MOSFET With Interface Fixed Charges, Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **The Second International Workshop on VLSI (VLSI 2011) in conjunction with (NECOM-2011)**, Venue: The Park Hotels, July 15 ~ 17, 2011, Chennai, India.
23. Drain Current Model of Nanoscale Dual Material Gate (DMG) MOSFET including interfacial hot-carrier-induced degradation effect", Mini, Vandana Kumai, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, International Conference on Microwaves, Antenna, Propagation and Remote Sensing, ICMARS-2011, Jaipur, India
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25. Temperature Dependent RF/microwave Characteristics of Nanowire Surrounding Gate MOSFET with Localised Charges, Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, International Conference on Nanoscience and Technology (ICONSAT – 2012), January 20 to 23, 2012 at Hyderabad, India.
26. Dynamic Performance Comparison of p-i-n and p-n-p-n Tunnel Field Effect Transistor and Impact of Gate Drain underlap , Rakhi Narang, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, International Conference on Nanoscience and Technology (ICONSAT – 2012), January 20 to 23, 2012 at Hyderabad, India.
27. Nano-scale Empty Space in Double Gate (ESDG) MOSFET for High Performance Digital Applications: A Theoretical Study, Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, International Conference on Nanoscience and Technology (ICONSAT – 2012), January 20 to 23, 2012 at Hyderabad, India.
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29. Comparative Study of Silicon On Nothing and III-V On Nothing Architecture for High Speed and Low Power Analog and RF/Digital Applications, Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, NANOCON 2012 – Second International Conference on Nanotechnology - Innovative Materials, Processes, Products and Applications during October 18-19 2012, at Bharati Vidyapeeth University, Pune, India, pp.105
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32. Modeling and Simulation of Nanoscale Lateral Gaussian Doped Channel Asymmetric Double Gate MOSFET, Vandana Kumari, **Manoj Saxena**, Mridula Gupta, NANOCON 2014 – Third International Conference on Nanotechnology during October 14-15, 2014 organized by Bharati Vidyapeeth University, Pune, India at Le-Meridien Hotel, Pune
33. pH sensing Characteristics of Silicon on Insulator (SOI) Junctionless (JL) ISFET, Ajay, Rakhi Narang, **Manoj Saxena** and Mridula Gupta, NANOCON 2014 – Third International Conference on Nanotechnology during October 14-15, 2014 organized by Bharati Vidyapeeth University, Pune, India at Le-Meridien Hotel, Pune
34. TCAD Assessment of Nanoscale Double Gate RingFET (DG-RingFET) Architecture: Analog and Linearity Performance Investigation for RFIC Design , Sachin Kumar, Vandana Kumari, **Manoj Saxena**, Mridula Gupta, NANOCON 2014 – Third International Conference on Nanotechnology during October 14-15, 2014 organized by Bharati Vidyapeeth University, Pune, India at Le-Meridien Hotel, Pune
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36. Linearity and analog performance realization of energy efficient TFET based architectures: An Optimization for RFIC Design, Upasana, Rakhi Narang, **Manoj Saxena** and Mridula Gupta, International Conference on Emerging Electronics (ICEE) held at J N Tata Auditorium, Indian Institute of Science during December 4-6, 2014
37. Modeling and Simulation of Nanoscale III-V based Tri Gate Stack MOSFET on Nothing for Improved Analog and Digital Applications, Vandana Kumari, **Manoj Saxena**, Mridula Gupta, International Conference on Recent Advances in Nanoscience and Nanotechnology (ICRANN-2014), Jawahar Lal Nehru University, New Delhi held during December 15-16, 2014
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39. Analysis of Cylindrical Gate Junctionless Tunnel Field Effect Transistor (CG-JL-TFET), Ajay, Rakhi Narang, Manoj Saxena and Mridula Gupta, 12th IEEE India International Conference, INDICON 2015, on Electronics, Energy, Environment, Communication, Computer, Control, (E3-C3) held during December 17-20, 2015 at Jamia Millia Islamia, New Delhi, India ***(Received Best Paper Award)*** (Presented)
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43. Physical Insights into Double Gate (DG) p-i-n TFET Operating States: Modeling and Simulation Study, Upasana, Sakshi Gupta, Rakhi Narang, Manoj Saxena and Mridula Gupta, 18th International Workshop on Physics of Semiconductor Devices (IWPSD 2015) held during December 7-10, 2015 at INDIAN INSTITUTE OF SCIENCE, Bangalore, India.
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45. Modeling and Simulation Study of Gate Material Engineered TFET Architecture Considering the Impact of Mobile Charge Carriers, Understanding Device Physics in Different Operational Regimes, Upasana, Rakhi Narang, Manoj Saxena and Mridula Gupta, 6th International Conference on Computers and Devices for Communication (CODEC-15) held at Swissotel Kolkata, India during December 16-18,2015.
46. Sub-threshold Drain Current Modeling of Tri-Gate Dielectric Pocket InGaAs-On-Nothing MOSFET, Vandana Kumar, Manoj Saxena and Mridula Gupta, International Conference on Devices, Circuits and Systems – ICDCS 2016 held during Mar 3-5, 2016 in Karunya University, Coimbatore, Tamil Nadu, India (Presented)
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3. Two-Dimensional Analytical Modeling and Simulation of Multiple Material Gate Oxide Stacked MOSFET, R. S. Gupta, Kirti Goel, **Manoj Saxena** and Mridula Gupta, **National Conference on Integrated Broad Band Digital Systems and Networks, NIEC**, Delhi, March 18-19, 2005

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4. RF Performance Investigation of Gate Stacked Insulated Shallow Extension (ISE) MOSFET and Bulk: A Comparative Study, Ravneet Kaur, Rishu Chaujar, **Manoj Saxena** and R. S. Gupta, **Proceeding of Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006)**, pp 254-258
5. Design and FPGA realization of Direct Sequence-Spread Spectrum (DS-SS) BPSK Modulator using a Five Stage Gold Code Generator, Rishu Chaujar, Ravneet Kaur, **Manoj Saxena** and R. S. Gupta, **Proceeding of Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006)**, pp 213-216.
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11. A 2-D Analytical Model for Gate Misalignment Effects on Graded Channel DG FD SOI n-MOSFET, Rupendra Kumar Sharma, **Manoj Saxena**, Mridula Gupta and R. S. Gupta, **Indian microelectronics Society Conference 2007 Theme: Trends in VLSI and Embedded System,** August 17-18, 2007, Punjab Engineering College, Chandigarh, India

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12. Development Board-Level Experimentation and Simulation of FPGA based DEBPSK DSSS Modulator: Implementation of 10-Chip Gold Code Sequence Generator, Rishu Chaujar, Ravneet Kaur, **Manoj Saxena** and R. S. Gupta, **Second National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2008)** September 26-28, 2008 in New Delhi, India, pp. 255-261.
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14. Solution to CMOS technology for high performance analog applications: GEWE-RC MOSFET , Rishu Chaujar, Ravneet Kaur, **Manoj Saxena**, Mridula Gupta, R. S. Gupta, **2nd National Workshop on Advanced Optoelectronic Materials and Devices, AOMD 2008**, art. no. 5075707, pp. 201-205.

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15. Effect of temperature variation on various parameters in Insulated Shallow Extension Silicon On Nothing(ISE-SON)MOSFET:A simulation study, Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **National Conference and Workshop on Recent Advances in Modern Communication Systems and Nanotechnology (**NCMCN – 2011), January, 06-08, 2011
16. Performance Comparison of Silicon and SiGe based Double Gate Tunneling Field Effect Transistor with gate stack architecture, Rakhi Narang, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **National Conference and Workshop on Recent Advances in Modern Communication Systems and Nanotechnology (**NCMCN – 2011), January, 06-08, 2011
17. Impact of Localised Charges on the performance of the Si Nanowire Surrounding Gate MOSFET, Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **National Conference and Workshop on Recent Advances in Modern Communication Systems and Nanotechnology (**NCMCN – 2011), January, 06-08, 2011
18. Investigation of Linearity Performance of a Double Gate Band to Band Tunnel Field Effect Transistor, Rakhi Narang, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **15th VLSI Design and Test Symposium***,* July 7-9, 2011, Wipro Technologies, Pune, India
19. Analog Performance of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: Simulation study, Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **15th VLSI Design and Test Symposium***,* July 7-9, 2011, Wipro Technologies, Pune, India
20. A Wide Temperature Range (50-500K) Analysis For Nanoscale Surrounding Cylindrical Gate MOSFET With Localised Charges, Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, **15th VLSI Design and Test Symposium,** July 7-9, 2011, Wipro Technologies, Pune, India

2012

21. Modeling and Simulation of Dielectric Pocket Silicon On Nothing (DiPSON) MOSFET, Neha Bhushan and **Manoj Saxena**, 99th Indian Science Congress held at KIIT University, Bhubneswar during Jan 03 – 07, 2012

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22. Impact of Insulating Layers on Single and Double Gate MOSFET for Improved Short Channel Effect and Hot Carrier Reliability , Vandana Kumari, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, First National Conference on Recent Developments in Electronics (NCRDE 2013), Department of Electronic Science, University of Delhi South Campus, New Delhi during Jan 18-20, 2013

23. High Performance Low Power 6T RAM Cell Using Gate-All Around (GAA) MOSFET , Rajni Gautam, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, First National Conference on Recent Developments in Electronics (NCRDE 2013), Department of Electronic Science, University of Delhi South Campus, New Delhi during Jan 18-20, 2013

24. Performance Investigation of Silicon Nanowire Tunnel FET for Analog and Digital Applications, Rakhi Narang, **Manoj Saxena**, R. S. Gupta and Mridula Gupta, First National Conference on Recent Developments in Electronics (NCRDE 2013), Department of Electronic Science, University of Delhi South Campus, New Delhi during Jan 18-20, 2013

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25. NI MULTISIM Implementation of Memristor Based Secured Communication System, Khushwant Sehra Poonam Kasturi Mamta Amol Wagh and **Manoj Saxena**, Proceedings of National Conference on Advancements in Electronics and Computer Applications NCAECA 2016 (UGC and DiETY Sponsored) held during Feb 04-05, 2016 at Shaheed Rajguru College of Applied Sciences, University of Delhi. Pp. 19-24, ISBN 978-93-5254-496-7 published by M/s Paramount Publishing House

Abstracts in National Conferences

1. Generation Of Arbitrary Waves Using Arduino Due, Arun Chahar, Poonam Kasturi and **Manoj Saxena** , Poster Presentation in THINK NANO 2016 – National Student Symposium organized by Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore held during March 31, 2016 - April 01, 2016 at IISc, Bangalore
2. Integration of Mem-Element with SCR based Rectifiers, Khushwant Sehra, Gaurav Kumar Shakya, Poonam Kasturi and **Manoj Saxena**, Poster Presentation in THINK NANO 2016 – National Student Symposium organized by Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore held during March 31, 2016 – April 01, 2016 at IISc, Bangalore
3. Simulation and Experimental Verification of Memristor Based XOR Gate, Arushi Gupta, Rishav Kumar Pandey, Divya Goel, Poonam Kasturi, Mamta Amol Wagh, **Manoj Saxena**, Poster Presentation in THINK NANO 2016 – National Student Symposium organized by Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore held during March 31, 2016 – April 01, 2016 at IISc, Bangalore
4. Smart Traffic System Design Based On PIC Microcontroller, Himanshu Bhardwaj, Samaa Manzoor Wani, Poonam Kasturi and **Manoj Saxena**, Poster Presentation in THINK NANO 2016 – National Student Symposium organized by Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore held during March 31, 2016 – April 01, 2016 at IISc, Bangalore

Conference Organization/ Presentations

Organization of a Conference

International Events

2004

Joint Secretary and Member - Technical Review Committee	16th Asia-Pacific Microwave Conference (APMC'2004), University of Delhi, December 15 - 18, 2004, New Delhi, India

2006

Member - Local organizing committee	India-Japan Workshop (IJW-2006) on ZnO Materials and Devices, December 18-20, 2006 sponsored by DST (New Delhi) - JSPS (Japan) organized by Department of Electronic Science, University of Delhi South Campus

2008	
Secretary	Mini-Colloquia on Compact Modeling of advance MOSFET structures and mixed mode applications on January 5-6, 2008 at University of Delhi South Campus, New Delhi, India sponsored by the IEEE Electron Device Society under its Distinguished Lecturer Program
2009	
Secretary	*The 18th WIMNACT(Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology)-New Delhi, India* - Mini-Colloquia on Compact Modeling and Fabrication techniques of advance MOSFET/ HEMT structures, June 04-05, 2009 at University of Delhi South Campus, New Delhi, India sponsored by the IEEE Electron Device Society under its Distinguished Lecturer Program
Symposium secretary	International Symposium on Microwave and Optical Technology (ISMOT)-2009 , December 16-19,2009 in Hotel Ashok, New Delhi, India
2011	
Program Committee Member	The Seventh International Conference on Distributed Computing and Internet Technology, Bhubaneswar, India, 9 – 12 February 2011
2012	
Program Committee Member	International Conference on Soft Computing for Problem Solving (SoCProS 2011), Roorkee, India, December 16-18, 2011 http://www.mirlabs.net/socpros11/
Convener	Science Academies Lecture Workshop On Frontiers in Science & Engineering - Opportunities for Graduates, February 17-18, 2012, SP Jain Centre Auditorium, University of Delhi South Campus, Benito Juarez Road, Dhaula Kuan, New Delhi
Member-Organizing Committee	International MOS-AK/GSA (India) workshop, March 16-17, 2012 in JIIT University, Noida, Uttar Pradesh, India
Member Technical Program Committee	Seventh International Conference on "Bio-Inspired Computing: Theories and Application, 2012 (BIC-TA 2012)" to be held at ABV-Indian Institute of Information Technology and Management Gwalior during December 14 - 16, 2012. http://www.iiitm.ac.in/bicta2012/
Secretary	**Mini-Colloquia** on **"Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis"** Organized by IEEE EDS-Delhi Chapter, New Delhi, India during **March 14-15, 2012 held at** SP Jain Centre Auditorium, University of Delhi South Campus, Benito Juarez Road, New Delhi, 110021. The Mini-Colloquia was sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program
Technical Program Committee Member	**10th International Conference on Distributed Computing and Internet Technologies, 6th - 9th February, 2014, Bhubaneswar, Odisha, India.**
Secretary	Mini Colloquia on "Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis" on January 13, 2015, University of Delhi South Campus
Member-Technical Program Committee	International Conference on 14th -15th Jan, 2016 themed on "Cloud System and Big Data Engineering" at Amity University Uttar Pradesh Noida Campus. http://www.gtie2016.com/committees.html#2

National Events

2003	
***Member* - Organizing Committee**	National Symposium on recent advances in microwaves and light waves (NSAML'03) University of Delhi South Campus, New Delhi, October 2003.
2005	
Treasurer and Member Organizing Committee	Short course on Spice Models for Advanced VLSI Circuit Simulation organized by Department of Electronic Science, University of Delhi South Campus, Dec. 11-12, 2005
2006	
Secretary and Member-Technical Programme Committee	National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2006) from **22nd March – 25th March 2006,** Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India
2008	
Co-convener and Secretary	National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008) from **26th September – 28th September 2008,** Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India
Coordinator	Two-Days Workshop On Quantum Mechanics: Theory and Application during **November 21-22, 2008,** Organized by Forum for Interdisciplinary Application in Sciences (FiDAS) Deen Dayal Upadhyaya College, University of Delhi, New Delhi Sponsored by Delhi Chapter of the National Academy of Sciences, India.
2009	
Co-convener and Secretary	Three days Workshop on Futuristic trends of Quality Control in Information Security Management, *Sponsored by CSIR, Govt. of India,* **October 09-11, 2009** organized by Forum for Interdisciplinary Application in Sciences (FiDAS) Deen Dayal Upadhyaya College, University of Delhi, New Delhi
Member-Organizing Committee	National Seminar and Workshop on Integrating Multiple Technologies to Support Teaching and Learning, **September 24-26, 2009** organized by Department of Electronics, Maharaja Agarasen College, University of Delhi and sponsored by UGC, Govt. of India
Coordinator	First One-Day National Workshop on Einstein & Special Theory of Relativity, *Sponsored By Delhi Chapter-National Academy of Sciences, India,* **November 06, 2009**
Coordinator	Second One-Day National Workshop on Einstein & Special Theory of Relativity, *Sponsored By Delhi Chapter-National Academy of Sciences, India,* **November 07, 2009**
Coordinator	Two-Day National Workshop on Fiber Optics and Applications, *Sponsored By Delhi Chapter-National Academy of Sciences, India,* **November 28-29, 2009**
2010	
Co-convener and Secretary	Third National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2010) held during **January 30-31, 2010,** Deen Dayal Upadhyaya College, University of Delhi, Shivaji Marg, New Delhi, India, *sponsored By University Grants Commission (UGC), Govt. of India*
Convener	First National Workshop On Recent Trends in Semiconductor Devices and Technology,

	Jointly Organized By Aryabhatta Science Forum, Deen Dayal Upadhyaya College, University of Delhi And IEEE EDS Delhi Chapter, New Delhi, *Supported By Integrated Microsystem, Gurgaon, India, Society for Microelectronics and VLSI*, New Delhi, **February 12-13, 2010**
Convener	Second National Workshop On Recent Trends in Semiconductor Devices and Technology, Jointly Organized By FiDAS, Deen Dayal Upadhyaya College, University of Delhi And IEEE EDS Delhi Chapter, New Delhi, Supported By DRDO, Govt of India and Integrated Microsystem, Gurgaon, India held during September 17-18, 2010
Convener	Second National Workshop On Quantum Mechanics: Theory and Application Organized By FiDAS, Deen Dayal Upadhyaya College, University of Delhi, Sponsored By CSIR, Govt of India Supported By IEEE EDS Delhi Chapter, New Delhi and The National Academy of Sciences, India, - Delhi Chapter held during Oct. 22-23, 2010 and October 29-30, 2010
2011	
Workshop Coordinator	Three Day Joint Science Academies Lecture Workshop On Frontier in Physics, January 21-23, 2011 jointly Organized by FIDAS, Deen Dayal Upadhyaya College and IEEE EDS Delhi Chapter at SP Jain centre, University of Delhi South Campus, New Delhi
Secretary	First National Workshop On Numerical Methods and Differential Equations in Computational Science (NUMDECS-2011), February 01-05, 2011 Organized by FIDAS, DDU College, Sponsored and Supported by University Grants Commission (UGC), Govt. of India
Member-Organizing Committee	*NATIONAL SEMINOR ON RECENT ADVANCES IN MICROELECTRONIC DEVICES* Organized by Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Sec-22, Rohini, Delhi-110086 sponsored by Defence Research and Development Organization Ministry of Defence, Government of India.
Convener	Science Academies Lecture Workshop On Frontiers in Science & Engineering - Opportunities for Graduates, February 17-18, 2012, SP Jain Centre Auditorium, University of Delhi South Campus, Benito Juarez Road, Dhaula Kuan, New Delhi
Convener	Science Academies Lecture Workshop On Joint Academies Lecture Workshop On History, Aspects and Prospects of Electronics in India, October 12-13, 2012, SP Jain Centre Auditorium, University of Delhi South Campus, Benito Juarez Road, Dhaula Kuan, New Delhi
Convener	Lecture Workshop on Trans-disciplinary Areas of Research and Teaching by Shanti Swaroop Bhatnagar Awardee, *February 01-02, 2013* organized by Deen Dayal Upadhyaya College, University of Delhi sponsored by Council of Scientific and Industrial Research (CSIR), New Delhi and supported by IEEE EDS Delhi Chapter
Convener	Third National Workshop On Recent Trends in Semiconductor Devices and Technology, January 19-20, 2013 Jointly organized by Deen Dayal Upadhyaya College, University of Delhi and IEEE EDS Delhi Chapter, New Delhi Sponsored By Defence Research and Development Organization (DRDO), Ministry of Defence, Government of India. Venue: SP Jain Centre, University of Delhi South Campus, Benito Juarez Road, Dhaula Kuan, New Delhi

Secretary	First National Conference on Recent Developments in Electronics (NCRDE 2013) is being organized by IEEE EDS Delhi Chapter. The conference will be held at Department of Electronic Science, University of Delhi South Campus, New Delhi during Jan 18-20, 2013
Convener	Fourth National Workshop On Recent Trends in Semiconductor Devices and Technology, September 12-13, 2014 organized by Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi Sponsored By Defence Research and Development Organization (DRDO), Ministry of Defence, Government of India.
Convener	On October 17, 2014, One Day Seminar on "Women in Science: A career in Science", Organized by Silizium-Electronics Society, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, supported by IEEE EDS Delhi Chapter and Science Education Panel, Indian Acdemy of Sciences, Bangalore
Convener	Second Lecture Workshop on Trans-disciplinary Areas of Research and Teaching by Shanti Swaroop Bhatnagar Awardee, January 30-31, 2015 organized by Deen Dayal Upadhyaya College, University of Delhi sponsored by Council of Scientific and Industrial Research (CSIR), New Delhi and supported by IEEE EDS Delhi Chapter
Convener	One Day Symposium to Celebrate International Year of Light held on October 28, 2015.

Participation as Paper/Poster Presenter

- A 2-D Subthreshold Analytical model for Short Channel Effects in Nanowire MOSFETs (Si, Ge), Gaurav Mahajan, Rakhi Narang, **Manoj Saxena**, V.K. Chaubey, **Nirma University International Conference on Engineering (NUiCONE) 2010,** December 09-11, 2010, Nirma University, Ahmedabad

Research Projects (Major Grants/Research Collaboration)

- **Co-Principal Investigator** in **UGC, Govt. of India** sponsored research project entitled Physics Based Modeling and Simulation of Channel Material Engineered Ring FET for Sensing Applications worth Rs. 17,23,000/-
  On Going - (October 01, 2015 - Till date)
- **Principal Investigator in a University of Delhi Sponsored Project under Innovation Project Scheme** entitled "Mathematical Modeling and Simulation of Circular and Non-Circular Gate Geometry Junctionless Nanoscale Transistor and co-integration with Memristor Based Electronic Circuits" worth Rs. 4,00,000/- .
  On Going - (October 01, 2015 - Till date)
- **Principal Investigator** in a **University of Delhi Sponsored Project under Innovation Project** Scheme entitled Analytical Modeling, Simulation and Verification of Emerging Nanoscale MULTIGATE Device Structures and Study of Government's Initiatives for Growth of Electronics In India, Project Code – 202 (2013) worth **Rs. 5,50,000/-**
  Completed - (November 2013 – February 2015)
- ***Co-Project Investigator*** in a **DST Sponsored Project** entitled *Analytical Modelling and Simulation of Sub-100 nm Advance Tunnel FET architecture for RF/ Microwave and Biosensing Applications*, (SR/S3/EECE/0062/2012) worth **Rs. 31,14,000.** Completed - (September 2012 – October 2014)
- ***Co-Project Investigator*** in a **DRDO sponsored Project** entitled *Analytical Modeling, Simulation and Characterization of Silicon Gate All Around Nanowire MOSFET for ULSI (Ultra Large Scale Integration) Circuit Applications* worth **Rs. 30,68,000.** Completed - (April 2012 – March 2015)
- ***Co-Project Investigator*** in a **DRDO sponsored Project** entitled Physics Based Modeling and Simulation of Sub-100 nm recessed channel (RC) and insulated shallow extension (ISE) MOSFET with gate electrode work function engineering structures for high performance applications (ERIP/ER/0803693/M/01/1258) worth **Rs. 4.70 lakhs**
  Completed - (October 2010 – July 2012)

- ***Co-Principal Investigator*** in **UGC, Govt. of India** sponsored research project entitled *Modeling and simulation of Nanoscale Dual Material Gate Insulated Shallow Extension Silicon on Nothing MOSFET for Low voltage low power applications* (F. No. 36-258/2008(SR)) worth **Rs. 9,22,800**. Completed - (May 2009 – April 2012)
- ***Co-Project Investigator*** in a **DRDO sponsored Project** entitled Physics Based Modeling Simulation and Electrical Characterization of a Novel Device Architecture: Silicon-On-Nothing MOSFET for Sub-100 nm Device Dimensions (No. ERIP/ER/0303417/M/01) worth **Rs. 31.68 Lakhs.** Completed - (April-2004-December 2007)

Awards and Distinctions

- Received ***Smt. Shanti Devi Bhargava Memorial Gold medal*** for being best candidate in the M. Sc Examination in Electronics in 2000
- Name appeared in the ***Golden List of IEEE Transactions on Electron Devices*** Reviewers for year 2005, 2006, 2008, 2009 and 2010.
- He was nominated as an *Expert in Electronics* for a TV Show on Delhi AAJ Talk held in June 2012
- Received outstanding EDS Volunteer recognition from EDS Chapters in the South Asia region in 2012.
- Received Meritorious Teacher by the Govt. of NCT of Delhi, India for the Year 2014, based on evaluation comprising of Student Evaluation, Result Evaluation, Self Appraisal and Evaluation by the Principal.

Association With Professional Bodies

Editing ---

Reviewing

- ***Reviewer*** of IEEE Transactions on Electron Devices
- ***Reviewer*** of Journal of Physics D: Applied Physics, Institute of Physics (IOP)
- ***Reviewer*** of Semiconductor Science Technology, Institute of Physics (IOP)
- ***Reviewer*** of Measurement Science and Technology (IOP)
- ***Reviewer*** of Solid State Electronics, Elsevier Science, UK
- ***Reviewer*** of Superlattices and Microstructures, Elsevier Science, UK
- ***Reviewer*** of International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, Wiley
- ***Reviewer*** of IET Micro and Nano Letters
- ***Reviewer*** of Journal of Electrical and Electronics Engineering Research (JEEER)
- ***Reviewer*** of MAPAN-Journal of Metrology Society of India
- ***Reviewer of*** International Journal of Science and Technology Education Research
- ***Reviewer of International Conference*** - *Asia Pacific Microwave Conference (APMC)-2008, 16-19, December 2008 in Hong Kong Convention and Exhibition Center, Hong Kong, China*
- ***Reviewer of International Conference*** - International Symposium on Microwave and Optical Technology (ISMOT)-2009,*16-19, December 2009 in Hotel Ashok, New Delhi, India*
- ***Reviewer for Book Proposal for Universities Press (India) Pvt. Ltd***. Hyderabad. (2009 -)
- ***Reviewer for*** The 8th International Conference on Computing, Communications and Control Technologies: CCCT 2010, Jointly with The 16th International Conference on Information Systems Analysis and Synthesis: ISAS 2010, In the Context of The International Multi-Conference on Complexity, Informatics and Cybernetics: IMCIC 2010, April 6th - 9th, 2010 Orlando, Florida USA
- ***Reviewer of*** National Conference on Recent Trends in Exotic materials (NCRTEM 10), Sharda University Greater Noida-201306, U.P., India
- ***Reviewer for*** 7th International Conference on Distributed Computing and Internet Technologies (ICDCIT – 2011), Bhubaneswar during 9 – 12 February 2011.

	• ***Member-Review Committee*** - International Conference on Latest Trends in Nanoscience and Nanotechnology (ICNSNT), 28th -29th March 2011, Karnataka, India • ***Reviewer of*** The SPRING 9th International Conference on Computing, Communications and Control Technologies: CCCT 2011 Jointly with The 17th International Conference on Information Systems Analysis and Synthesis: ISAS 2011 In the Context of The 2nd International Multi-Conference on Complexity, Informatics and Cybernetics: IMCIC 2011, March 27th - 30th, 2011 ~ Orlando, Florida USA • **Reviewer for** The 4th International Multi-Conference on Engineering and Technological Innovation: IMETI 2011, July 19th - July 22nd, 2011 – Orlando, Florida, USA • ***Reviewer of*** International Symposium on Models and Modeling Methodologies in Science and Engineering: MMMse 2011 in the context of The 15th World Multi-Conference on Systemics, Cybernetics and Informatics: WMSCI 2011, July 19th - July 22nd, 2011 – Orlando, Florida, USA
Advisory Committees and Boards	• Member of Editorial Board of International Scholarly Research Network (ISRN) Electronics - http://www.isrn.com/32538140/ • Expert Member - Directory of researchers working in the country in the area of Nano Science and Technology, Nano Mission, Department of Science and Technology, Govt. of India • Member of Selection Committee - Engineering Sciences for selection of students and faculty members at National level for SRF programme. • Jury Member in 3rd National Level Exhibition and Project Competition (NLEPC), DST, Govt. of India, October 08-09, 2013, New Delhi • Jury Member in 4th National Level Exhibition and Project Competition (NLEPC), DST, Govt. of India, October 06-08, 2014, New Delhi • Jury Member in 5th National Level Exhibition and Project Competition (NLEPC), DST, Govt. of India, December 06-07, 2015, New Delhi • Member-Faculty of Interdisciplinary and Applied Sciences, University of Delhi (2016) for a period of 3 years
Memberships	• Vice Chair – IEEE EDS SRC Region 10 • Regional Editor IEEE EDS Newsletter – Region 10 South Asia • Senior Member – IEEE, USA (July 2008 -) • MIET - Member – Institution of Engineering and Technology (IET), United Kingdom (UK) (2008-) • Member - International Association of Engineers, Hong Kong • MInstP - Member – Institute of Physics (IOP), (May 2011 -) • Member of Editorial Board of International Scholarly Research Network (ISRN) Electronics • Expert Member - Directory of researchers, Nano Mission, DST, Govt. of India • Associate – Indian Academy of Sciences (IAS), India (2009 – 2012) • M. N. A. Sc – Member, National Academy of Sciences India (NASI), Allahabad, India (2009 -) • Life Member – Semiconductor Society of India, New Delhi, India • Life Member - Indian Science Congress Association (ISCA)
Office Bearer	• Chapter Advisor – The National Academy of Sciences, India – Delhi Chapter (2016 -) • Secretary – IEEE EDS Delhi Chapter, New Delhi, India (2010 – Till date)

	• Secretary - Institute of Physics (UK)- Delhi Chapter (2013 - 2014) • Executive Committee Member – IET(UK) Delhi Network (2013 - 2014) • Joint Secretary – Society for VLSI and Microelectronics, New Delhi, India (2008- Till date) • Joint Secretary and Treasurer – IEEE EDS Delhi Chapter, New Delhi, India (2009)
Other Activities	
Workshop/ Seminars/ Conferences Attended: • Indian Academy of Sciences, Platinum Jubliee Meeting, Bangalore, **November 12-14, 2009** • Bhabha Centenary Symposium, Tata Institute of Fundamental Research, Mumbai, India, **December 03-05, 2009** • Indian Academy of Sciences 76th Annual Meeting 2010**, Goa, 12 to 14 November 2010**	

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